73. The microprocessor system of claim 72 further comprising: means to produce a "TRUE" or "FALSE" outcome from the testing of a condition, said response to a SKIP instruction modified to occur when said outcome is "TRUE."

74. The microprocessor system of claim 71 further comprising:

a loop counter that is connected to receive a decrement control signal from instruction decoding means;

instruction decoding means that are configured to supply a reset using said counter control signals to said counter and a decrement control signal to said loop counter in response to a MICROLOOP instruction in said multiple sequential instructions.

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75. The microprocessor system of claim 74 further comprising: means to produce a "TRUE" or "FALSE" outcome from the testing of a condition, said response to a MICROLOOP instruction modified to occur when said outcome is "TRUE."

76. The method of claim 74 modified to not supply said reset using said counter control signals to said counter if, as the result of a decrement using said control signals, said loop counter is zero.

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77. The microprocessor system of claim 71 further comprising instruction decoding means that are configured to supply a reset using said counter control signals to said counter and to supply control signals to said instruction fetching means such that a subsequent fixed-length instruction group is supplied to said instruction register and to supply the remainder of said fixed-length instruction group as an operand in response to a variable-length-operand-using instruction in said multiple sequential instructions.

78. The microprocessor system of claim 71 further comprising instruction decoding means that are configured to supply a last byte of said fixed-length instruction group as an operand in response to a last-byte-operand-using instruction in said multiple sequential instructions.

79. The microprocessor system of claim 71 further comprising instruction decoding means that are configured to supply control signals to said instruction fetching means such that a subsequent said fixed-length instruction group is supplied as an operand in response to a extra-group-operand-using instruction in said multiple sequential instructions.

80. The microprocessor system of claim 71 further comprising instruction decoding means that are configured to supply control signals to said instruction fetching means such that the next said fixed-length instruction group supplied to said instruction register is determined in response to a branch-type instruction in said multiple sequential instructions.

81. The microprocessor system of claim 77 or 80, wherein said branch-type instruction is a variable-length-operand-using instruction.

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82. The microprocessor system of claim 80 further comprising the supplying of a reset using said counter control signals to said counter in said response to a branch-type instruction.

83. The microprocessor system of claim 80 further comprising a means to produce a "TRUE" or "FALSE" outcome from the testing of a condition, said response to a branch-type instruction modified to occur when said outcome is "TRUE."

84. The microprocessor system of claim 71 wherein said instruction fetching means fetches said multiple sequential instructions in parallel for said fixed-length instruction group in a single memory cycle.

85. The microprocessor system of claim 71 further comprising:

memory access testing means for testing the current said instruction group to determine if the multiple sequential instructions require a memory access; and